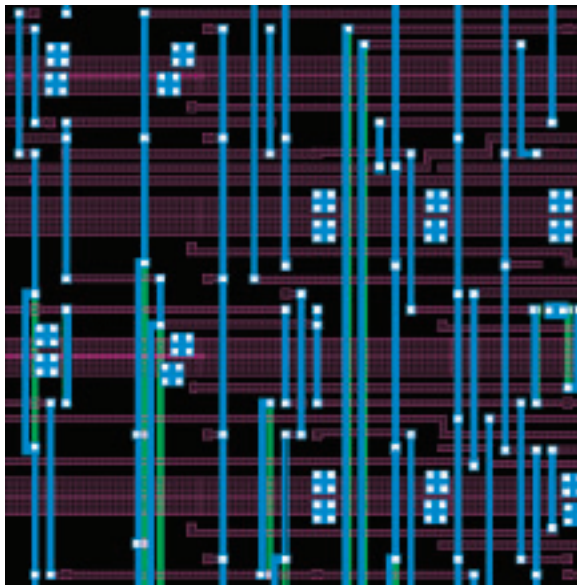


**SiFix™**

Automatically finds and corrects physical violations in technology and reliability design rules resulting in shorter implementation time and improved manufacturing yield.

The increasing use of advanced, subwavelength geometry process technologies for integrated circuit (IC) manufacturing has created a gap between the detailed physical design rule requirements and the ability of current design tools and methodologies to implement these rules correctly and quickly. This gap results in delayed implementation, delayed tape-outs, excessive tape-out efforts, as well as creating reliability and manufacturability issues in the final silicon chip.



**SiFix scans a physical design** and automatically finds and corrects physical violations in technology, reliability or methodology design rules. SiFix can be used to address and fix a large quantity and variety of process and design violations, including:

- DRC fixes and updates due to late process revisions
- Via doubling and enlarged metal coverage to enhance reliability and yield
- Yield enhancement by implementing relaxed design-rule values where possible
- Clean up DRC violations left by automatic routing or layout synthesis software
- Selective net-oriented wire segment widening and via insertion for enhanced reliability

SiFix reads and writes standard industry formats and interfaces smoothly and easily with existing design and tape-out environments. It operates directly on the Cadence DFII design database or on final GDSII data,

originating from either full-custom or cell-based design methodologies, for both digital and analog designs.

**Benefits**

- Fast, automatic implementation of physical DRC corrections
- Shortens total physical implementation time
- Allows design implementation to start early before final design rule values are available
- Improves design immunity to yield issues through implementation of relaxed rules
- Fixes reliability hazards by widening, spacing and increasing connectivity of selected wires and wire segments
- Local-limited operation ensures no need for extraction and timing re-verification

**Features**

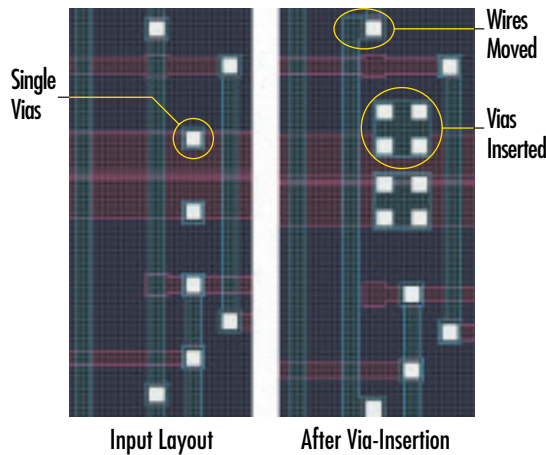
- Works on final GDSII data to fix final tape-out issues
- Minimal disturbance – shapes move by one grid only, if sufficient
- No change to the overall size and footprint
- Design hierarchy and structure kept intact
- High capacity – up to full chip
- Graphical reporting of design issues before/after corrections
- Direct DFII interface – preserves all connectivity, attributes, properties and P-cells
- Easy to use – users define only what needs to be changed
- Changes limited to single masks, if required
- Changes can be limited to selected cells only

# SiFix

The creation of mask layout data is typically a “two-steps forward and one-step backward” process, requiring designers to re-edit or touch up parts that were already considered complete. With the latest process generations, an increasing amount of post-design edits are necessary before the final mask layouts can be taped out. These edits range from tool-induced DRC errors, through DRC errors created by later process revisions, to yield and reliability enhancements.

SiFix provides an automated solution for implementing such corrections and enhancements. SiFix identifies errors and corrects them with minimal impact to the original design. SiFix is able to handle very large amounts of data (up to entire chips), and because of its limited and localized operation, the resulting layout does not need to go through another extraction and timing verification iteration.

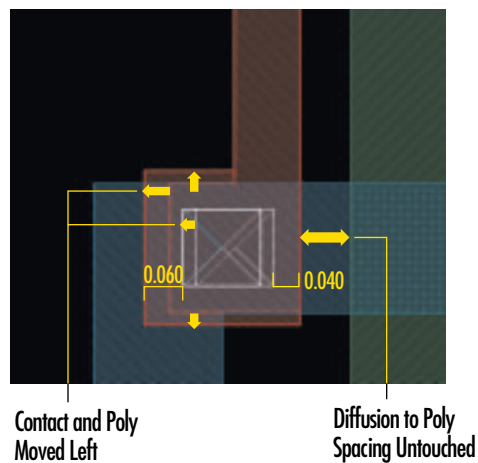
**Figure 1**  
*Vias inserted for enhanced manufacturability*



## Application 1 Via insertion for improved manufacturability

In a flash-memory device, designed and manufactured by a leading semiconductor memory manufacturer, the number of vias on long wires needed to be increased by more than double. SiFix accomplishes this task by creating room in the routing to accommodate the additional vias and only moves wires slightly when necessary.

**Figure 2**  
*Detail:  
SiFix implementation of larger poly-contact extends, without modifying diffusion mask*



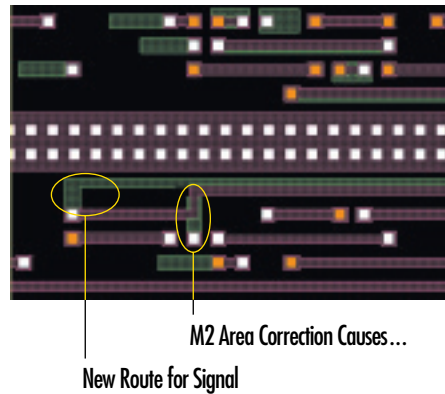
## Application 2 Yield enhancement

Design rule manuals increasingly prescribe to the need for using relaxed design rule values on locations where the design density will allow it. For the latest generation of processes, this requirement has become mandatory – designing physical layouts to be DRC-correct is no longer a guarantee they can be manufactured successfully. SiFix is able to automatically implement such relaxed design rule values on selected cells and masks, making it a vital step in a Design for Manufacture (DfM) design flow.

Figure 2 shows an example of how the poly-extend around a contact is enlarged by SiFix by only modifying poly and contact masks. Shown is the result from SiFix overlaying the input – only slight modifications have been made to the polysilicon and contact masks to implement a larger contact coverage. Because the diffusion mask had to remain identical, the contact has been moved slightly to the left.

### Application 3 DRC-fixing

Close to the tape-out deadline, the target foundry for an ASIC product changes the design-rule spec: enlargement of the metal2 minimum area rule value. Existing mask layouts now need to be enhanced for this new rule, preferably without a timing closure iteration involving physical synthesis and timing verification. SiFix accomplishes this task by modifying only metal2 in the routing level; leaf cells and all other masks are untouched.

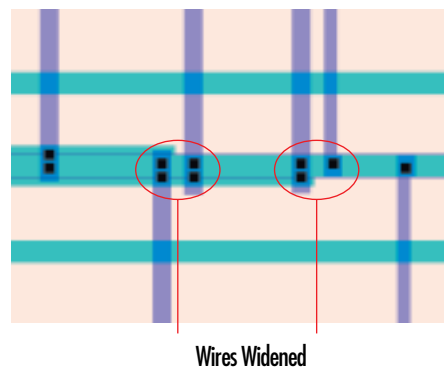


**Figure 3**  
SiFix cleans M2 area violations; modified M2 indicated in green and changed areas are highlighted in yellow

### Application 4 Reliability improvement

To improve reliability in a high performance, full-custom datapath design, certain selected wire segments needed to be widened to accommodate the increasing current densities of these specific nets. SiFix was able to implement the wire widening requirements by making only very local changes around the wires identified by the user.

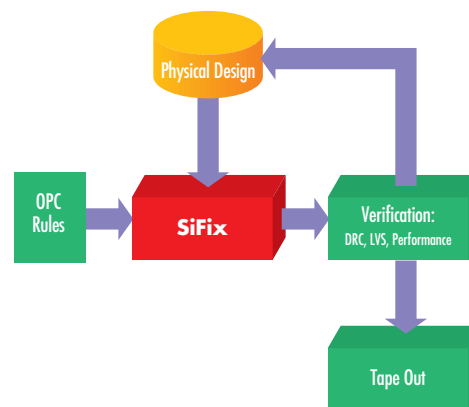
Figure 4 shows the SiFix results, where the central line has been widened at the indicated locations and additional vias were inserted to account for the increased current density. The dashed wire indicates the original route of this net. As more wires are connected to the net, a wider route is necessary to sustain the cumulative current.



**Figure 4**  
Wire widened by SiFix to account for increased current density

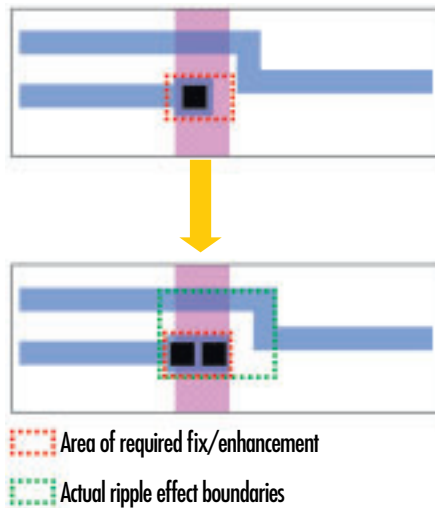
### Application 5 Optical proximity correction (OPC) rules implementation

Certain OPC requirements, like enhanced spacing to wide metal bars, are better implemented during the layout design-stage than during an OPC layout processing, just before mask generation. The benefits are the possibility to fully verify the functionality and performance of the enhanced design and less polygon fracturing resulting in much smaller databases. Instead of adding this task to the already full plate of the physical designer, SiFix can be introduced as part of the design verification flow to automatically implement these OPC requirements.



**Figure 5**  
Design flow for implementation of OPC rules with SiFix

**Figure 6**  
SiFix changes create a minimal disturbance



## Under the hood

SiFix has a unique capability of implementing enhancements on large designs, and only a minimum disturbance is needed to achieve each enhancement. Each single error location is visited, and polygon edges from user-selected masks and cells are locally moved to the extent needed, by only one process grid if possible. Every occurrence through the design hierarchy is instantly evaluated, thereby preserving DRC and LVS correctness of the total design. Designers have observed that SiFix operates very similarly to how manual fixes and adjustments are done, but it is orders of magnitude faster and does not introduce new violations. It frees them to spend more time on design architecture, creation and analysis work.

As a member of the SiClone™ product family, SiFix shares many of the capabilities well known in SiClone: a unique, n-level hierarchical layout processing tool that poses no restrictions on hierarchy structure, cell placement and overlays, and shapes of cells. In particular, constructs like programming via-cells, L-shaped cell boundaries and fully overlapping cells, are internally represented as such by the engine. This allows SiFix to make adjustments to specific cells, while respecting constraints from all instantiations of that cell-master at the same time. SiFix specifically does not rely on any cell or window abstraction methodologies, instead it is able to judge the impact a particular design change has on the full layout – a task which is very difficult and extremely laborious to do manually.

Joining SiClone and Hurricane™, SiFix shares a complete integration with existing design and verification methodologies based on GDSII or Cadence DFII databases. Since all attributes and properties of a design can be maintained, SiFix is optimally suited to fit into existing IC design flows.

For updates on software compatibility and supported platforms, check on the web at: [www.sagantec.com](http://www.sagantec.com).

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