

SiClone™

Accelerate Physical Implementation and Closure for Full Custom Design

Simultaneous, n-level hierarchical layout compaction, process migration and physical optimization.

SiClone is an automation solution for full-custom layout design. It accelerates the physical implementation of custom circuits by reusing existing, proven physical design. It executes rapid process migration by carefully repositioning all layout elements and polygon edges such that the resulting layout is design rule correct and optimized for its design performance targets.

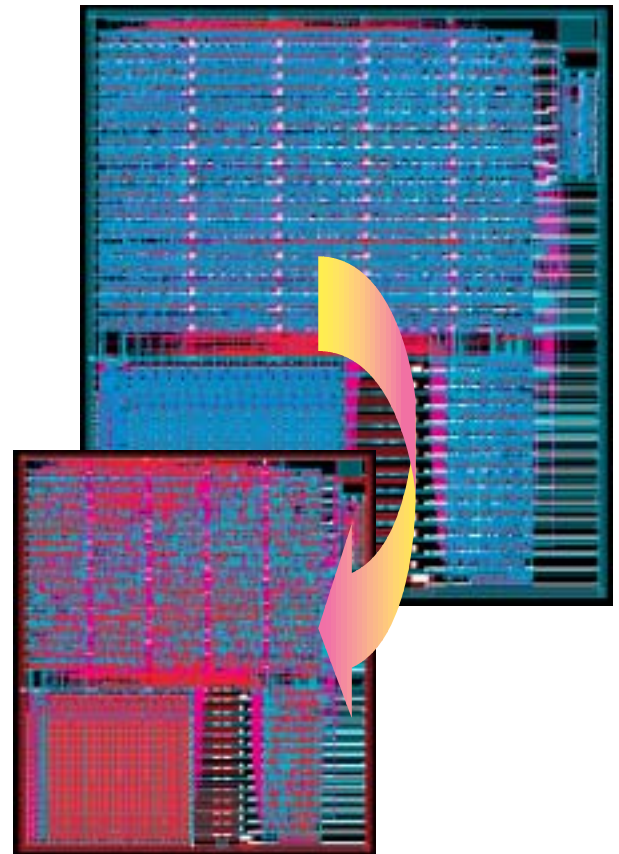
Typical target customer designs include high-performance logic design for CPU and DSP cores, embedded and dedicated memory designs as well as analog/mixed-signal circuits. Operating on GDS2 data or directly on your Cadence DFII database, SiClone automates the manual work of preparing mask layouts for next generation products. Thus the resource-intensive and time-consuming task of physical implementation and retargeting of full-custom designs can be automated by SiClone, thereby reducing design-cycle time, lowering design cost and enabling fast design closure and improved circuit timing and power performance.

Features

- Complete, n-level, physical hierarchy compacted simultaneously
- Original physical hierarchy structure kept intact to match schematic and netlist hierarchy
- Device sizes automatically adjusted from schematic, netlist or table
- Automatic optimal adjustment of contact straps for resized transistors and well/substrate ties
- Full control over width and spacing of power lines and individual signals
- Automatic via doubling
- Direct DFII interface: connectivity, properties and attributes maintained
- Supports advanced deep sub-micron technology design rules
- Intelligent selective application of multiple-value, DFM design rules

Benefits

- Faster time-to-market for any full-custom physical design implementation
- Design database and verification environment kept intact
- Fast design closure for timing, power and reliability
- Physical design optimization for improved timing and power performance targets
- Handcrafted density and quality, superior to any layout migration shrink methods

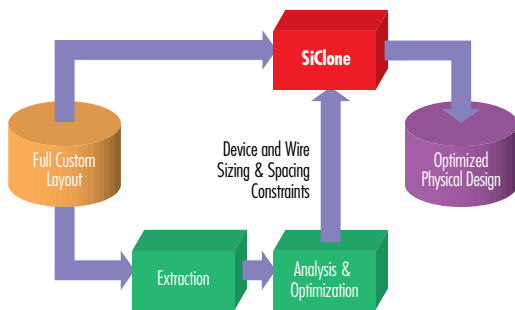


Application Design Closure and Performance Optimization

High performance and low power designs require optimal matching of every transistor's drive-strength to its respective net load. SiClone enables such automatic matching by accurately sizing every physical transistor in the design. In a design closure flow, after initial physical implementation, all actual net loads are accurately extracted from the layout. Static timing or timing simulation validate timing of all critical paths. In case timing violations are detected, transistor sizes on critical paths are adjusted by SiClone to fix such timing issues.

In a performance optimization application, a netlist with actual loads can be optimized for higher timing and power performance targets by circuit optimization tools. These tools reach these user-specified performance targets by increasing drive of timing critical netlist devices and reducing sizes of non-critical devices. These new device size values are then fed to SiClone for automatic layout adjustment.

Using this flow designers have increased clock frequency by 20% and decreased power consumption by 15%, all in one pass.



Design Closure and Performance Optimization Flow

Wide Range of Applications

SiClone has been used successfully in different areas of the IC-design spectrum – all sharing the common requirement that full-custom design is an essential methodology to achieve their targets for functionality, density and performance. SiClone has enabled many design teams to produce better layouts at advanced technologies in significantly shorter time.

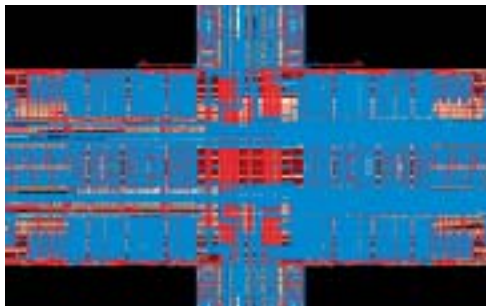
Actual Solution Examples

Circuit: DRAM control logic and I/Os

Product: 256 Mbit DRAM IC

Objective: Technology migration

Rapid, automatic migration of a complete control circuit of a 256 Mbit DRAM, including pads, fuses, and various analog sub-blocks from a 0.20 micron process to the latest technology.

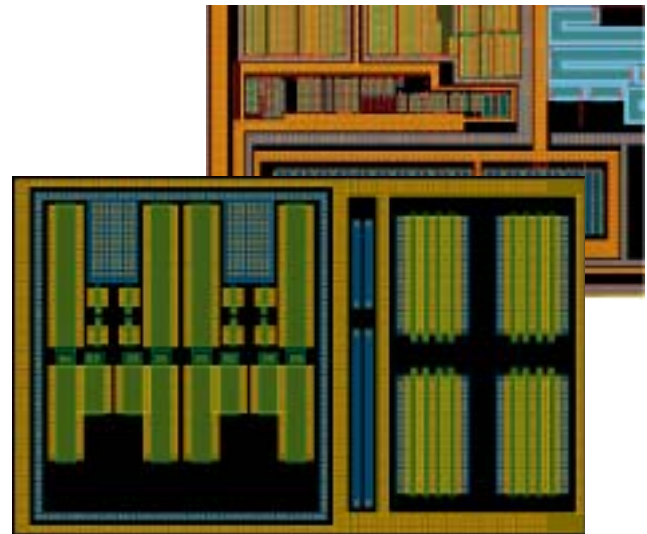


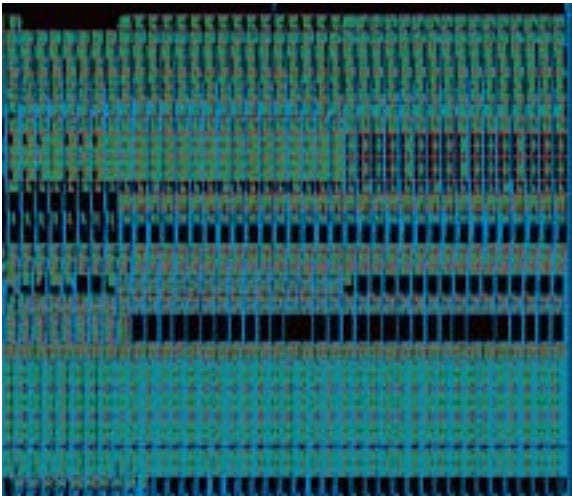
Circuit: PC I/O and USB2 interface

Product: PC chipset

Objective: Technology migration

Automatic process migration of a mixed signal PC I/O and USB2 interface circuit. Handling symmetry and matching requirements and the correct sizing of capacitors and resistors.



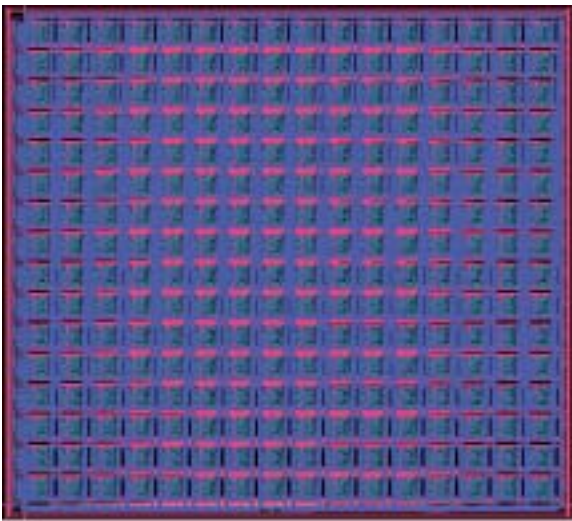
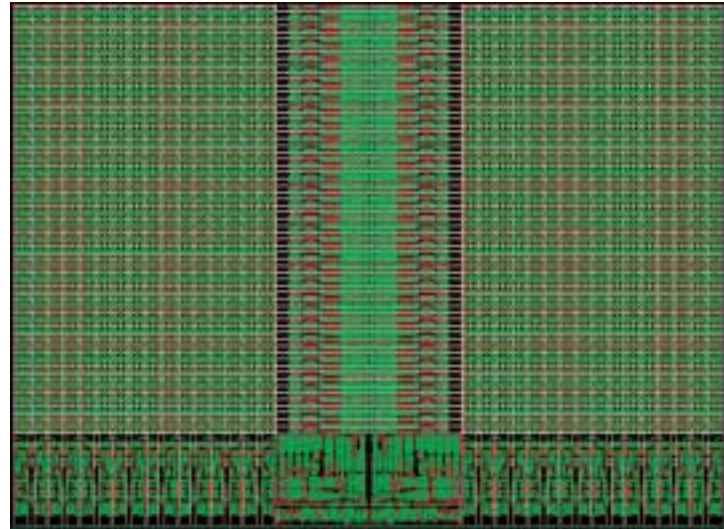


Circuit: Memory Compilers
Product: ASIC and SoC design library for 0.13 micron technology
Objective: Technology migration

The driving force for memory IP designers is to be able to rapidly support new emerging processes even before the process design-rules are stable. This allows their customers to tape-out simultaneously with the release of the process. Automatic process migration with SiClone enables them to meet this target.

Circuit: High-performance, low-power datapath and custom logic
Product: Low-power GHz microprocessor
Objective: Optimization and design closure for timing and power.

Accomplished 20% timing performance increase and 15% power consumption decrease at the same time, by automatic optimized adjustments of device physical sizes on critical and non-critical timing paths.



Circuit: Embedded FPGA circuit
Product: Communication SoC
Objective: Technology migration

Technology migration of a FPGA embedded block as part of the physical implementation of a low power telecommunication device. FPGA designs are dense, deeply-hierarchical, full custom structures. SiClone rapidly converted the entire embedded block to the target technology with optimal density.

Underlying Unique Technology

Under the hood of SiClone, is the first and only commercial simultaneous, n-level hierarchical layout compaction engine. A layout compaction engine works like a DRC-checker that not only finds the rules in a given physical layout, but also makes all rule-distances their specified minimal value to achieve maximum design density. With an n-level compaction technology, the physical hierarchy is not only maintained but also processed in its entirety. During simultaneous hierarchical processing, SiClone calculates the smallest possible design size, by in-parallel optimization of every unique cell-master for all its instantiations. This technology allows layout migration, for the first time, to be an integral part of physical design flow. It maintains consistent structure across all design representation levels, with no need to modify existing design and verification environments. It allows automatic physical migration to take part in the 'live' and incremental nature of IC design that is manageable, changeable and re-usable.

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