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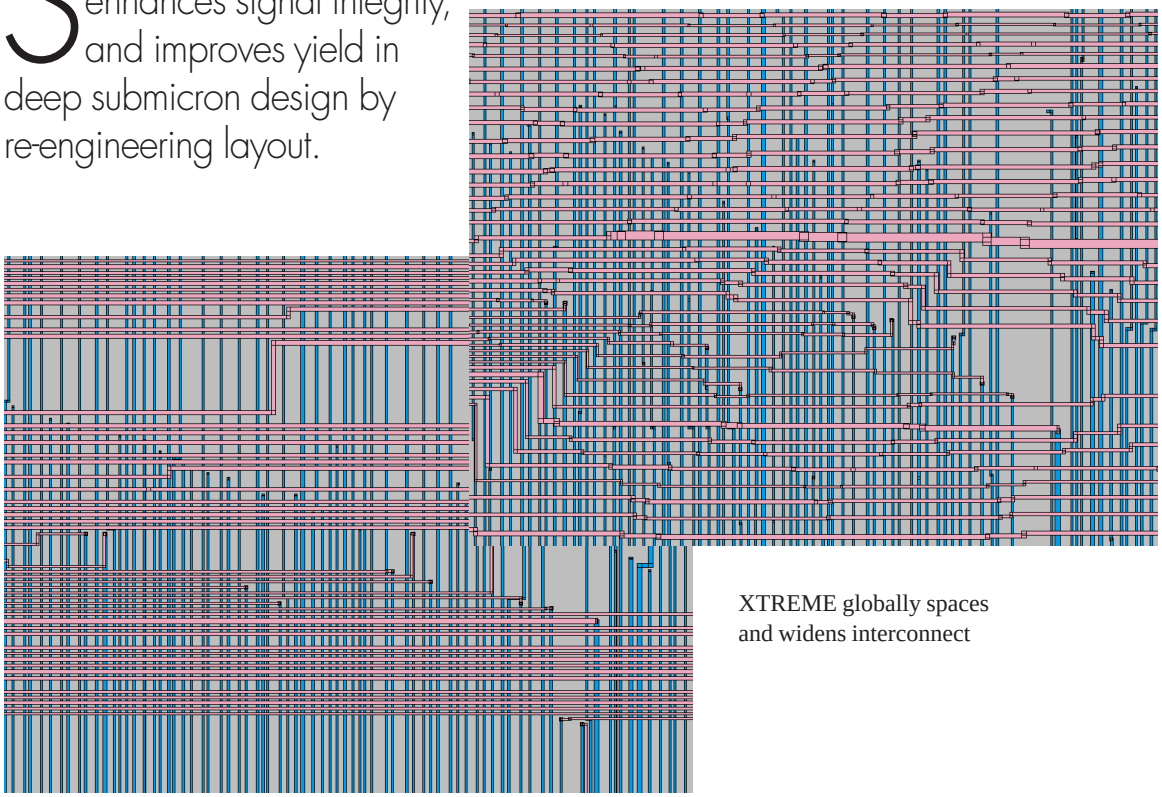
XTREME™

X-Talk-Reduced, Manufacturing-Enhanced

Significantly reduces crosstalk, enhances signal integrity, and improves yield in deep submicron design by re-engineering layout.



XTREME globally spaces and widens interconnect

Features

- User defined, net specific or globally spaces and widens interconnect
- Handles any number of interconnect layers
- Supports a variety of routing styles
- Preserves hierarchy and connectivity
- Interfaces with industry standard place and route tools using LEF/DEF
- Interfaces with industry standard signal integrity and noise analysis tools
- Accepts shape and symbolic data
- User controlled option for automatically doubling of via
- Provides full control of spacing and wiring tradeoff
- Handles large million gates designs

Benefits

- Reduces crosstalk by more than 50 percent
- Increases manufacturing yield and reliability
- Increases signal integrity
- Reduces power consumption
- Improves performance

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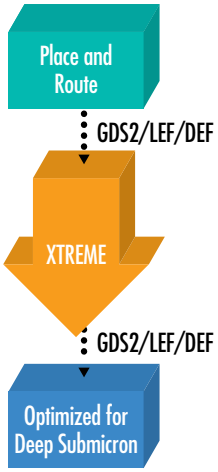
XTREME

Overview

XTREME is state of the art physical design and layout re-engineering software. It significantly reduces crosstalk, increases manufacturing yield and reliability, improves performance, and reduces the power in high-performance deep submicron design (DSM) without redesign or process technology changes. After routing has been completed, XTREME analyzes the design for crosstalk, and then globally spaces and widens the routing wires to minimize crosstalk and improve performance and reliability.



Deep Submicron Design Solutions

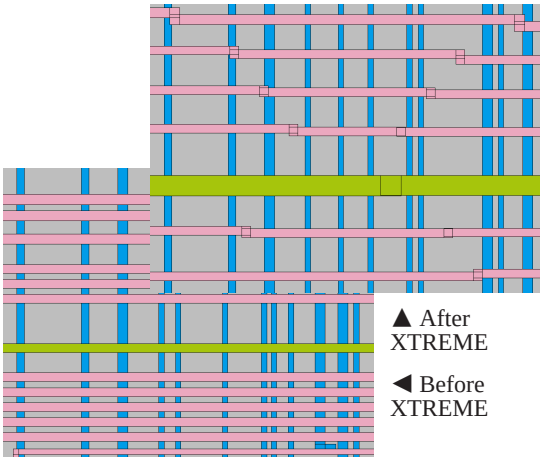
Noise from crosstalk in deep submicron designs can severely impact functionality, performance and reliability. As feature size shrinks and density increases, line-to-line capacitance and signal integrity become worse. Line-to-line capacitance within the same layer and signal integrity are major problems in deep submicron designs of 0.35 and below. For 0.35 micron designs, the coupling capacitance can be up to 70 percent of the total interconnect capacitance; for 0.18 micron designs, the coupling capacitance can exceed 90 percent of the total interconnect capacitance. XTREME is an ideal solution for these problems in full custom and semicustom, high-performance designs.

Already employed by engineering teams designing leading processor technology, XTREME is used for new or existing designs of 0.35 micron and below. It reduces cross-coupling capacitance by 40 percent for 0.35 micron designs, and by more than 50 percent for 0.25 micron and below. It improves the performance of DSM designs without redesign or changes to the process technology or silicon area.

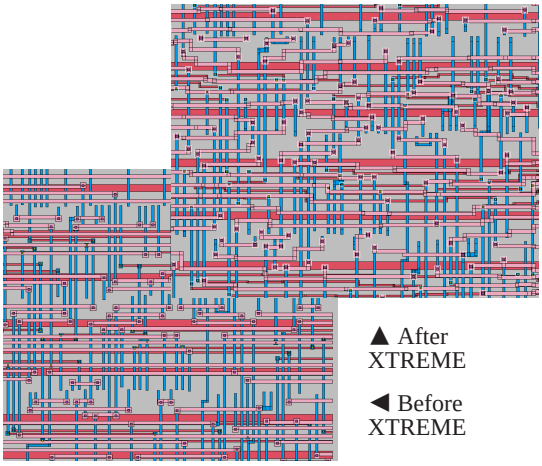
Layout Re-Engineered for Deep Submicron

XTREME is employed after routing, preferably before manual layout changes, checking and extraction. It is best used for every functional block once its routing is finished, and then for top-level routing.

XTREME spaces and widens wires globally or net specific on all metal layers to minimize crosstalk without increasing the silicon area, giving the designer full control over critical nets. XTREME pays special attention to predefined signals with extra spacing or wire widening. It improves metal coverage of contacts and increases the number of cut holes whenever possible. XTREME handles hierarchy and any number of layers, while preserving connectivity and design rule correctness. It accepts shape and symbolic data, and supports net specifications. XTREME supports a variety of routing styles, including sea-of-gates, channel based or data path.



Interconnect spaced and widened with XTREME



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