

# Anaconda™

Accelerate analog physical design by reusing existing topology and applying constraint-driven layout compaction

## Overview

Most of the time and effort in analog physical design is spent on the tedious detail work at the device, wire and polygon level. Many final instances of circuit and layout share a similar topology and are differentiated only by device parameters and second-order geometric details. Most of the time, to design a new cell, topologies do not need to be created but rather preserved and reused while geometry details are tweaked and refined for each specific circuit. Examples include manually re-sizing devices and wires again and again in order to match certain output loads, or migrating the design to other processes, meeting symmetry and matching requirements. Automation applied to these geometry modifications can have a major impact on overall analog design productivity.

Anaconda allows designers to reuse existing layout topologies and implement modified device parameters and design constraints from a schematic – minimizing layout time and effort. Figure 1 illustrates the impact of Anaconda on the overall analog design cycle. By migrating an initial design to create a new baseline topology in the target technology and then shortening the refinement time for each derivative design, Anaconda users can accelerate analog physical design time by a factor of three or more.

By maintaining a pre-determined and well-designed layout topology, Anaconda provides a controlled mechanism to accelerate layout – yielding results with the predictability and quality of hand-crafted layout. Furthermore, Anaconda is seamlessly integrated into the Cadence® Virtuoso® schematic and layout environment. Anaconda can be used immediately to augment and accelerate existing flows and methodologies whether traditional analog layout or automatic layout synthesis tools are being used.

## Constraint-Driven Operation

From an easy-to-use yet powerful graphical user interface designers can add constraints in both schematic and layout views (see Figure 2) thereby annotating the design database with design intent. Anaconda then updates the layout according to schematic device parameters and additional design constraints to create a refined and final DRC and LVS correct layout.

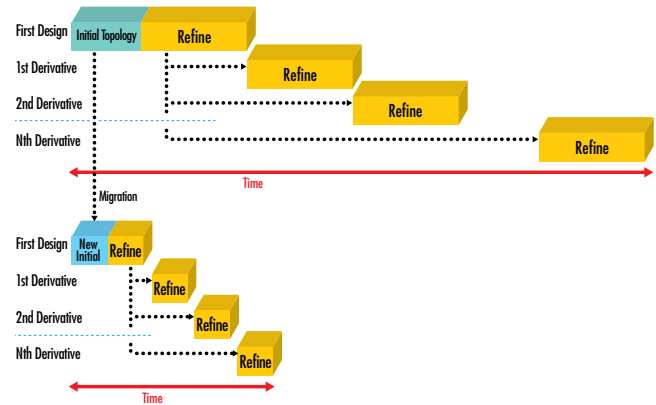


Figure 1 – Manual vs. Anaconda Design Time

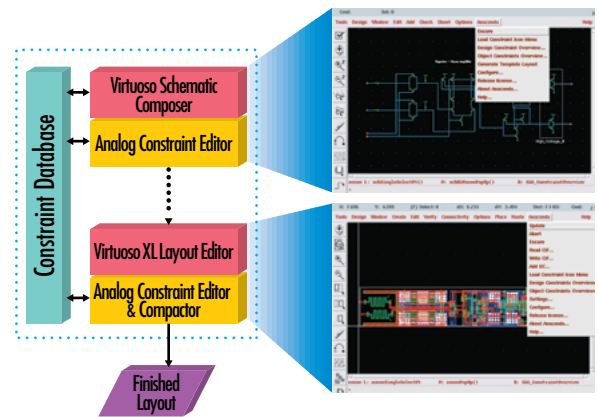


Figure 2 – Schematic-Based, Constraint-Driven Flow

## Features and Benefits

- Automates and accelerates the process of optimizing or creating derivatives from an existing layout topology
- Handles all geometric details: device placement and parameters, symmetry, wire widths, matching, alignment, etc.
- Constraint driven, with schematic-level capture and automatic layout implementation
- Connectivity-aware device replacement from schematic
- Results are DRC and LVS correct
- Allows reuse of both schematic and layout topologies
- Integrated with Cadence Virtuoso-XL design environment
- Supports Virtuoso database, structures and attributes
- Available on Solaris, HP-UX and Linux platforms

## Template-Based Layout Design

In analog design, circuit functionality and performance are extremely sensitive to physical implementation details. Therefore, it is critical that a layout be optimally implemented. This begins with a well-chosen topology or architecture followed by carefully crafting all physical details. Since reaching optimal circuit behavior is an incremental task, designers need to have complete control at each step of the implementation thereby enabling predictable results.

A simple and proven methodology to achieve these goals is to use well-designed templates for each type of circuit. Such a layout template includes all the circuit devices and objects and the connectivity.

The relative placement and orientation of these elements has been carefully chosen in the template. The properties that are going to be modified for each derivative implementation are the actual device parameters, sizes and wire dimensions. The template is flexible enough to accommodate variations in device parameters and overall cell dimensions but maintains the basic layout characteristics that were chosen for this family of circuits.

With Anaconda, designers can update their schematic using the constraint-driven layout compaction engine with connectivity-aware device replacement. Changes will be automatically implemented at the layout level using the base template, resulting in a completely predictable, hand-crafted quality layout that is correct by construction (see Figure 3).

This template-based methodology makes Anaconda an ideal tool for implementing high-performance analog layout that is crafted with maximum control and precision.

Figure 4 shows final physical implementations of three different circuits that are all derived from the same basic template using different device parameters.

## Integration with Standard Platforms and Flows

Anaconda is seamlessly integrated into the Cadence Virtuoso Custom IC Design System and allows for interactive editing of both schematic and layout views. It supports Cadence Virtuoso and Virtuoso XL, and Composer schematic editor. Anaconda maintains all Virtuoso data elements, properties and attributes with complete support for schematic driven Pcell-based designs.

Anaconda accelerates and augments existing design flows - rather than trying to replace them. At the same time, connectivity-aware device replacement offers more flexibility and productivity compared to direct device-size updating from a

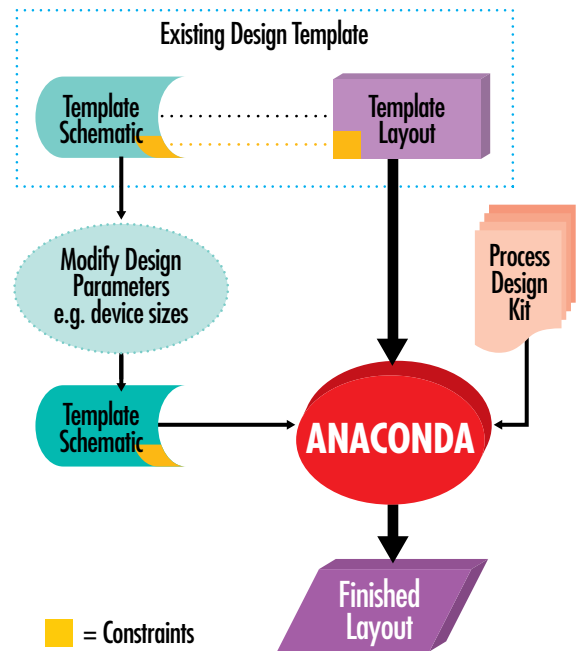


Figure 3 – Template-Based Design Flow



Figure 4 – Three Derivatives from One Layout Topology (Template)

schematic. It ensures correct and predictable results with complete designer control.

Analog designers are in full control throughout the process and they can make incremental changes at any time. For example, implementing an ECO will result in the appropriate local change rather than a complete redesign of the entire layout.

Anaconda is the newest member in the Sagantec family of production-proven custom layout tools. With Anaconda, Sagantec now offers designers a comprehensive and integrated solution for reusing, migrating and accelerating high-performance analog designs.

Sagantec  
North America, Inc.  
46485 Landing Parkway  
Fremont, CA 94538  
Tel: 510 360-5200  
Fax: 510 360-5255

Sagantec Israel Ltd.  
3. Hayozma Street  
P.O. Box 117  
Tirat-Carmel, Israel 39100  
Tel: (+972) 4 857 2781  
Fax: (+972) 4 857 2848

Sagantec Netherlands  
Eindhoven Towers, 4th Floor  
5611 CA Eindhoven  
P.O. Box 2102  
5600 CC Eindhoven  
Tel: (+31) 40 297 3773  
Fax: (+31) 40 297 3770

email: [info@sagantec.com](mailto:info@sagantec.com)

[www.sagantec.com](http://www.sagantec.com)

©Sagantec 2003.  
All Rights Reserved,  
Sagantec North America.  
All trademarks are the property  
of their respective owners.