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PHYSICAL DESIGN: PROCESS MIGRATION

Analog Hard IP Made Portable

Automating the flow for porting mixed-signal
IC designs across processes and foundries

By Malcom Macintosh

The fast moving and highly competitive datacomm markets require increased levels of integration, frequent upgrades, and technology shrinks. Datacomm integrated circuits (ICs) usually comprise multiple functional blocks and sub-circuits—digital, mixed-signal, and analog. The mixed-signal and analog portions of these IC products are the most difficult portions of the chip to migrate between foundries and technology nodes. Each communication port requires a physical layer transceiver, and one chip may have multiple communication ports and different communication busses such as Ethernet or USB.

Conexant Systems, Inc. (Newport Beach, CA) is a global provider of integrated semiconductor products for communications applications including cable, satellite, terrestrial data and digital video networks. Like many companies, Conexant outsources its silicon fabrication, using multiple CMOS processes at several major foundries. Frequently, the different foundries are not fully aligned at the same process technology node, so designs are often alternated between foundries and processes. Often, we need to migrate an existing design from one foundry to another. In many cases we simultaneously perform a technology shrink to achieve higher clock speeds, lower power consumption, smaller die size, and lower chip cost. All of this requires a careful and detailed choreography.

Conexant has developed a new process-portable design flow for mixed-signal chips. Using that flow, we successfully implemented a simultaneous foundry and technology migration port of a mixed-signal circuit from a 0.25-micron implementation at one major foundry to a 0.18-micron implementation at a different foundry, and achieved first-pass functional silicon.

MIGRATING BEYOND MANUAL

Most Conexant mixed-signal designs use internally developed proprietary intellectual property (IP) blocks that take considerable time and effort to develop and verify. To maximize our design investments, we reuse blocks and hard IP whenever possible. Not having to recreate a complex circuit saves months of design, layout, and verification time. In addition, the quality advantage of using a known, fully characterized, and field-tested design greatly reduces the risk of errors and costly surprises.

We found it difficult, however, to realize our reuse goals using traditional manual layout methods. Although these methods met our exacting performance requirements, it was taking a team of designers/layout engineers several months to port a typical Ethernet physical (PHY) block to a new process. Porting involves iterating layout design changes, extraction, and simulation until the desired characteristics are met. In addition, if design changes are required after simulation, further manual modifications are required in the layout phase.

Given the size and complexity of each migration and the number of required migrations within a short period of time, we concluded that traditional porting methods were too time-consuming and costly. Our challenge, therefore, was to create a design flow that would enable us to reuse the same IP blocks, shrink them without losing the circuit characteristics, and port them to a different foundry process easily and quickly.

Our main objective was not to automate or replace the front-end circuit design effort as the circuit was previously designed and proven. We needed, instead, to build a

flow that would use the existing circuit and automate the adjustment of the layout to fit the established design objectives, while maintaining the same layout architecture and structure as much as possible. The methodology we chose had to meet various fundamental requirements, and most importantly, it had to fit seamlessly into our current design environment.

PORTING PROTOCOL

Our custom design flow is built around custom design tools from Cadence Design Systems, Inc. (San Jose, CA), including the Cadence Virtuoso XL environment. Virtuoso XL provides a connectivity based design flow that integrates the schematic and layout design and makes use of programmable cells (Pcells) to allow designers to generate and update basic devices such as NFET and PFET. The Virtuoso XL system enables the building and maintaining of Pcells, as well as the storage of many abstract objects, relations, and annotations in a Cadence proprietary Virtuoso XL database. Thus our design team had a number of requirements to consider when establishing the design flow.

First, the porting between processes had to be done using the Virtuoso XL database, so that design kit libraries, Pcells, database objects, and attributes were consistently maintained. The critical link between schematic and layout also had to be maintained to ensure that the layout and schematic hierarchies are equivalent. Second, the methodology had to bridge between the two different processes in terms of layer mapping and device mapping; to take advantage of Virtuoso XL, the device mapping had to be based on our Pcell methodology. Third, we had to consider the fact that many devices would need to be tuned and resized to match

the circuit specification. The methodology had to support physical device resizing and automatic adjustment of the layout 'neighborhood' around each modified device.

A fourth and final requirement of the flow was to maintain the critical analog physical design constraints and layout properties such as device mirroring and symmetry, alignment, and routing matching. We looked at several options here, one being layout synthesis from a netlist. It was rejected, however, because that technique attempts to accelerate the original creation of a new layout in opposition to design reuse and migration. Since one of our major goals was to try to preserve the original physical design, analog synthesis tools were therefore not an appropriate choice.

Another option we considered was to shrink the layout to the new dimensions and then manually fix the remaining design rule violations. That, however, precipitated the need to resize the devices and modify or recreate them and estimates indicated it would be very layout design intensive. The post shrink layout effort would be hard to predict for any type of migration. Additionally, this methodology option would not be scalable and could not support multiple design closure iterations.

Ultimately we chose to use automatic layout migration and compaction tools—the SiClone migration engine and Anaconda analog-driven compaction from Sagantec (Fremont, CA). These tools are powerful and smart enough to do the back-end porting job based on original layout and new schematic data and constraints. These tools also interface well with the Cadence platform, so we could create a porting flow fully compatible with our existing Virtuoso

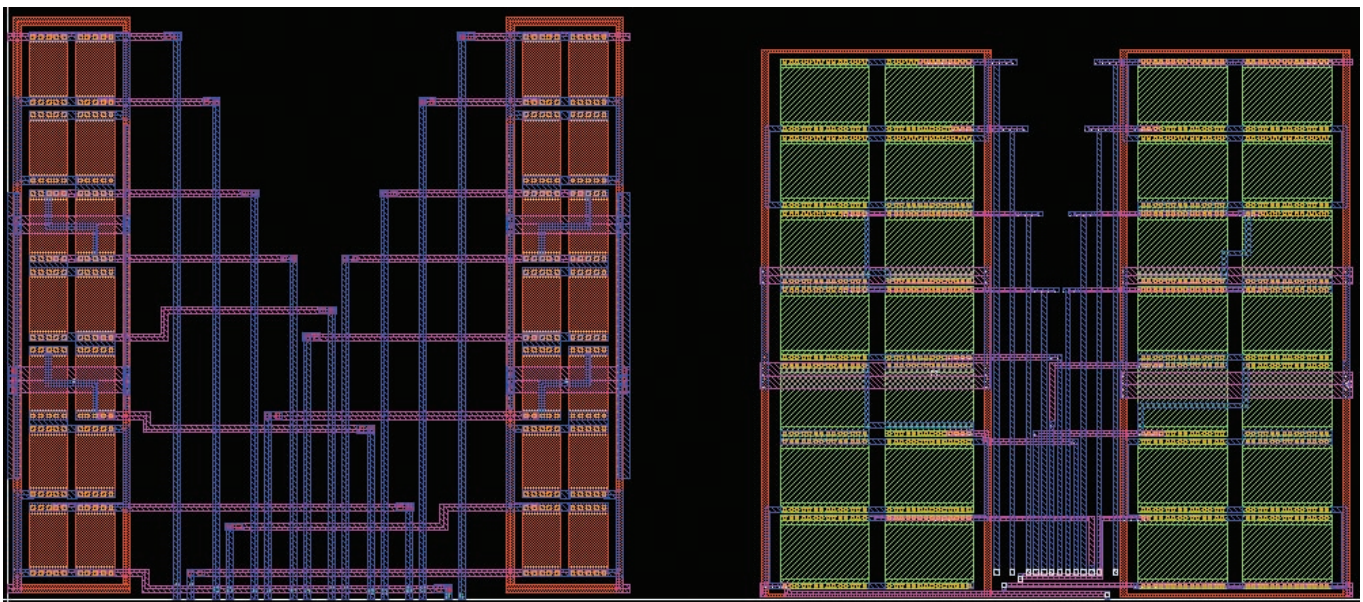


Figure 1: Process migration includes mapping to different device implementations and resizing. Here, diffusion resistors in the source process are replaced by different size poly resistors in the target process.

XL environment and all its features. The Sagantec tools can deal with most of the layout design work automatically, adjusting the basic layers and design rules according to the target technology file. They adjust devices and wires based on parameters and constraints annotated in the schematic, thus supporting a correct-by-construction design porting methodology.

Finally, one of the most difficult goals—and the most important feature—was the ability to swap devices from one technology to another, or within the same technology. SiClone handles instance-based device swapping using a target process design kit (PDK) library. These features proved crucial time savers, as our particular migration required swapping devices in the target technology (e.g., HVNFET to NFET, diffusion resistors to poly resistors) due to voltage source changes and device performance. (See Figure 1)

THE DESIGN MIGRATION FLOW

The result of our efforts is a successfully implemented design migration flow that addresses our multiple criteria, principally having the design data fully implemented in Virtuoso XL. A Virtuoso XL-consistent database ensures a persistent link between schematic and layout, and the Pcell implementation makes it much easier to do circuit and sizing changes. Once a design is Virtuoso XL-compliant, it is far easy to maintain any circuit changes between schematic and layout to verify LVS (layout versus schematic) consistency. Our methodology also achieves hierarchy equivalence between schematic and layout. (see Figure 2)

The migration itself starts by resizing a schematic to match the target foundry process. Since the source and destination processes have different minimum design rules and different electrical parameters, their size parameters need to be completely adjusted. We try to maintain the topology as much as possible and accommodate all changes by device sizing only. Initial sizing is done using a script that must be followed with careful simulation and verification. A few iterations of sizing and simulations may be required to get each device to its optimal size.

At any given time, a resized schematic can be automatically turned into a resized and optimized layout based on existing layout topology using the SiClone migration tool. With SiClone, any original foundry process (Foundry A, 0.25-micron PDK) Pcell instance can be replaced with a new Pcell instance at the target foundry process (Foundry B, 0.18-micron PDK) using the target schematic parameters. Once the instances are replaced, compaction takes place to accommodate the new instance dimensions. We then compact the entire layout and make sure it obeys the new process design rules (DRC) and that the layout matches the simulated schematic (LVS). The layout is extracted and the parasitic annotated netlist is fed back to simulation for verification and possible fine-tuning.

If architectural changes are required—but no resizing or DRC changes needed—then such changes are made in the schematic, and simulations are run to verify the changes. Resizing iterations can be tried (for ‘free’) and schematic engineering change orders (ECOs) made until

Conexant Automatic Process Migration Flow

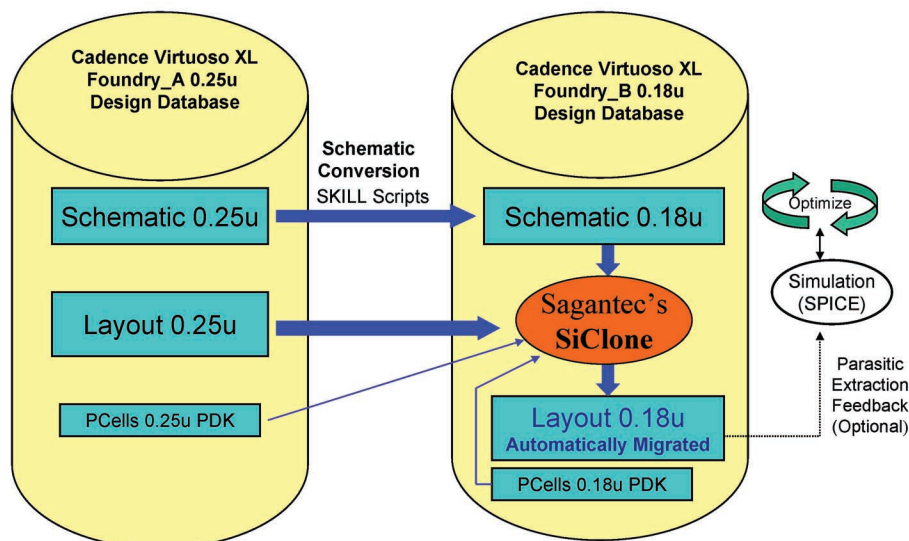


Figure 2: The process migration flow from Foundry A to Foundry B retains the physical topological information, while automatically adjusting the polygons to match the target process design rules.

the simulation performance meets requirements. Layout migration then follows and again the design comes out both LVS and DRC clean.

Using the flow, the entire design and migration process is much easier and faster and, while it preserves the layout structure as much as possible, architectural changes are still possible—an especially important criteria when dealing with external IP. The migrated layout is entirely Virtuoso XL compatible, so the IP is completely reusable for the purpose of design changes, integrations, or the next process port.

We have found this migration flow delivers very predictable results both in terms of quality and schedule, and is also scalable to different technologies and larger designs. In fact, the entire layout process is fully automatic and driven from circuit front-end design changes. The total migration time is much shorter than in any previous flow and, hence, more design iterations are possible (for optimizing and resizing). Parasitic extraction (PEX) results can be used to modify the design more quickly, since changes can be made and layout can be generated quickly and correctly to implement and verify the changes.

EVIDENCE OF SUCCESS

The first circuit to use the flow was the PHY portion of our standard Ethernet interface, which is used in many of our products. For this migration, we executed a simultaneous foundry and technology port of the PHY circuit from a 0.25-micron process implementation at one foundry to a 0.18-micron process implementation at a different foundry. After deploying the flow, the migrated IC had a successful tapeout. Functional silicon has arrived back from manufacturing, which has closed the loop and provided final confirmation of success.

The result of this automatic flow implementation demonstrates a substantial calendar-time and cost savings over previous traditional porting methods. We have successfully eliminated the time-consuming design/layout/redesign iterations. The flow now is automatically driven by the circuit design and simulation tasks, the whole porting effort now 'front-end bounded.'

Whereas previously, a large portion of a layout designer's time was spent pushing polygons and fixing DRC errors, now we are using SiClone and Anaconda to perform these laborious and mundane tasks automatically. Our layout designers can focus more effectively on higher-level tasks, boosting their productivity and the quality of results.

As a result of these efforts, today we are performing automatic front-end driven layout. Designers can simulate with layout information that has been created and extracted quickly. It is possible to complete our designs more quickly and unlike many predecessor analog methodologies, both the front end and back end can converge within days of top-level verification.

By providing automatic flows to Conexant design teams, we allow our engineers to be creative while protecting both the success and schedule of our product. Moving forward to even smaller geometry technologies, these flows will prove to be invaluable in addressing the many issues that can compromise design schedules. Following this current successful implementation, we intend to use the strategy for many future designs and migrations to 0.18-micron, 0.13-micron, and 90-nanometer process technology nodes across multiple foundry sources. ♦

As a Design Automation Engineer at Conexant Systems, Malcolm Macintosh is responsible for integrating and developing new automated methodologies for analog/mixed signal design. Before joining Conexant, Mr. Macintosh was a Layout Designer at Mosaid Technologies. He lives and works in San Diego, CA.

The logo for Sagantec features the company name in a bold, lowercase, sans-serif font. A horizontal line with a red-to-yellow gradient runs through the middle of the letters 'a' and 'n'.

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