Sagantec's *nm*igrate adopted and deployed for 14nm technology

Major semiconductor company successfully migrated 28nm libraries to 14nm FinFET

Santa Clara, California - May 29, 2013 - Sagantec announced that its ***nm*igrate** tool was adopted by a major semiconductor company for the development of standard cell libraries at 14nm and 16nm FinFET technologies.

This customer already used *nm*igrate successfully to migrate a library from a 28nm technology implementation to another foundry 14nm FinFET process. The migration from planar 28nm to 14nm FinFET is very challenging, since it needs to deal with new interconnect layers, satisfy stringent restrictions on front-end layers and FinFET device constraints, new MOL structures and rules and double patterning coloring rules. The *nm*igrate tool deploys an automated two-dimensional, dynamic layout compaction technology which optimally enforces all the above design rules and constraints and delivers a 100% DRC clean and optimal result.

In addition to using *nm*igrate as a layout migration tool, *nm*igrate is also used for DRC clean up and design rule updates. In this use model, layout designers draw or modify layout manually, and use *nm*igrate for final DRC cleanup. This semi-automatic use model provides significant design acceleration and effort savings, and is particularly beneficial in 14nm and 16nm technologies where manual layout design takes much more effort than in previous nodes.

Availability

The *nm*igrate migration and compaction tool is already available for customers who wish to accelerate the layout design work of libraries in 14nm and 16nm process nodes, or would like to migrate existing planar 28nm or 20nm libraries to 14nm or 16nm FinFET technologies.

This year at DAC

*nm*igrate migration and DRC-cleanup presentations and demos at the 50th Design Automation Conference in Austin TX, can be scheduled here

About Sagantec

Sagantec is the leading EDA provider of process migration solutions for custom IC design. Sagantec's EDA solutions enable IC designers to leverage their investment in existing physical design IP and accomplish dramatic time and effort savings in the implementation of custom, analog, mixed-signal and memory circuits in advanced process technologies.
These solutions have been used commercially by tier-1 semiconductor companies, and have

been proven to reduce layout time and effort by factors of 3x to 20x and enable dramatically faster introduction of IC products in new technology nodes.
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