

## Sagantec and TSMC Collaborate on Sagantec DFM-Fix

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October 25, 2007 -- **Sagantec, Inc.** has announced the results of its ongoing work with Taiwan Semiconductor Manufacturing Company to provide new automated capabilities for lithography hotspot correction at advanced process technology nodes with DFM-Fix. DFM-Fix speeds turnaround time by automatically addressing hotspots in all critical layers at all design levels, including key building blocks such as library, memory, IP and custom blocks. It also provides automated handling of post-implementation hotspots caused by boundary proximities and inter-level effects.

Currently available fixing flows address hotspots in higher metal layers and at the routing implementation level. With DFM-Fix, designers can automatically correct hotspots in all layers, as well as hotspots caused by inter-cell placement or interaction between IP and routing. This expands automated DFM correction encompasses the whole chip, at every design level and for every mask layer.

TSMC and Sagantec tested DFM-Fix on multiple complete designs with hotspots in various layers. In all test cases, DFM-Fix automatically corrected most of the hotspots, with correction rates of 95% and above in most cases. The flow also proved highly time-efficient, running all test cases in under three hours on a standard quad-CPU platform.

## About DFM-Fix

DFM-Fix uses information generated by lithography analysis to identify hotspots and correct them in the physical design database. DFM-Fix corrects the physical shapes with minimal impact on the design. At the core of the product is a hierarchical layout optimization engine that makes subtle polygon movements at minimum increments, and maintains design rule check (DRC) compliance while performing model-based optimization. The subtle geometry corrections made by DFM-Fix make a big difference for the lithography and manufacturing process, but are below a meaningful threshold for electrical extraction and timing analysis. DFM-Fix can move and size any wire, edge and shape to required location, size and width to fix the hotspot while maintaining DRC correctness of all related polygons across all relevant layers and hierarchy levels. If the only way to fix a hotspot is by violating a design rule, the user can specify their preference and priority. A sign-off DRC tool should be run to confirm the design rule integrity prior to tape-out.

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**Keywords:** Sagantec, TSMC (Taiwan Semiconductor Manufacturing Company), design for manufacturing, design-for-manufacturing, DFM, EDA tools, ASIC design,

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